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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,386	02/18/2004	Michael Peters	022193-042810US	4341

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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/782,386	PETERS, MICHAEL	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 29-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,29-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 4, 7 – 11, 28 – 36 and 39 – 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Barth *et al.* (US Patent No. 5,747,914, hereinafter "Barth").

3. With respect to claims 1, 11 and 28 – 31, 34, 39 – 42, Barth discloses a method for reading data from a synchronous memory (see col. 2, lines 10 – 32, and col. 7, line 66 – col. 8, line 11, teachings apply to DRAMS in general including EDO and SDRAM) of the type having data cells arranged in rows and columns and having a single row cache (figure 6, 604, 608), comprising:

arranging said synchronous memory in a symmetrical layout (figure 7) to include a left plurality of N memory portions including a left memory block (708A), a central sense amplifier block (704), and a right memory block (702A); a centrally located single row cache (704); and a right plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block, wherein N is at least equal to two (708B, 706, 702B);

receiving an initial command and row address data for reading contents of a row of said memory selected by said row address data, said reading being performed exclusive of column address data (col. 6, lines 27 – 31);

moving said contents of said row into said single row cache (col. 6, lines 30 – 31);

after said contents of said row have been moved into said single row cache, receiving a "read" command and column address data; and

in response to said "read" command, reading data from said single row cache at a column address specified by said column address data for output by said memory (col. 6, lines 31 – 35).

4. With respect to claims 2 – 4, 7 – 10, 32, 33, 35 and 36, the limitations recited in these dependent claims relate to operations of conventional DRAMs that are not novel features of the claimed invention. For example, substantial concurrency between a command and data addresses is a general feature of a conventional DRAM as is the latency of memory outputs. Bank activation and precharging are also present in conventional DRAMs.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 11 and 28 – 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dosaka et al. (US Patent No. 5,680,363, hereinafter "Dosaka") in view of Kundu (US Patent No. 5,692,148).

7. With respect to claims 1, 11 and 28 – 31, 34, 39 – 42, Dosaka discloses a method for reading data from a memory (figure 22) of the type having data cells arranged in rows and columns and having a single row cache (SMA 1 – 4), comprising:

arranging said synchronous memory in a symmetrical layout to include a left plurality of N memory portions (LMB) including a left memory block, a central sense amplifier block (dark region between LMB and UMB, see also figure 28, 504 and col. 6, lines 11 – 13), and a right memory block (UMB); a centrally located single row cache (SMA 1 – 4, SRAMs comprise at least one row or register, an SRAM cache register also holds data from one row of DRAM, col. 5, lines 11 – 13); and a right plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block, wherein N is at least equal to two (figure 22);

receiving an initial command and row address data for reading contents of a row of said memory selected by said row address data (col. 13, lines 28 – 30), said reading being performed exclusive of column address data (col. 5, lines 10 – 19, transferring the entire row of data transferred simultaneously does not require any column address, see also col. 5 lines 28 – 50) ;

moving said contents of said row into said single row cache (col. 5, lines 11 – 13);

after said contents of said row have been moved into said single row cache, receiving a "read" command and column address data; and

in response to said "read" command, reading data from said single row cache at a column address specified by said column address data for output by said memory (col. 5, lines 20 – 23).

Dosaka disclose all of the limitations discussed above. However, Dosaka does not specifically disclose that the memory is of synchronous DRAM type. On the other hand, Kundu specifically discloses that synchronous DRAMs (SDRAMs) are faster than DRAMs (Kundu, col. 1, lines 36 – 39).

It would have been obvious to one of ordinary skill in the art, having the teachings of Kundu and Dosaka before him at the time the invention was made, to use the faster SDRAM teachings of Kundu in the memory system of Dosaka, in order to reduce memory access cycle by almost 50% (Kundu, col. 1, lines 39 – 42).

8. With respect to claims 2 – 4, 7 – 10, 32, 33, 35 and 36, the limitations recited in these dependent claims relate to operations of conventional DRAMs that are not novel features of the claimed invention. For example, substantial concurrency between a command and data addresses is a general feature of a conventional DRAM as is the latency of memory outputs. Bank activation and precharging are also present in conventional DRAMs.

9. With respect to claims 5, 6, 37 and 38, outputting data from memory after two clock cycles is specifically shown in figure 4a of Kundu. In addition, a person having ordinary skill in

the art would have found it obvious to output data from memory after a specific number of clock cycles in accordance with the characteristics desired.

Response to Amendment

10. Claims have been amended to overcome a previous rejection under 35 USC, 112, second paragraph and to correct informalities introduced in the preliminary amendment filed February 18, 2004. Corresponding rejection is withdrawn. As to the informalities introduced in the preliminary amendment, the Examiner does not believe that any additional corrective measure, other than this amendment, is required.

Response to Arguments

11. Applicant's arguments have been fully considered but are moot in view of the new ground(s) of rejection.

12. As to Applicant's argument regarding the rejection of claim 10 under 35 USC 112, second paragraph, contrary to Applicant's assertion, claim 4 has not been amended to overcome the rejection.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
October 31, 2005